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EXAMINER	
SZETO, JACK W	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,522	JEDDELOH, JOSEPH M.	
	Examiner	Art Unit	
	Jack W. Szeto	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/19/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Official Action

Status of the Specification and Claims

Claims 1, 15, and 28 are rejected under obviousness-type double patenting.

Claims 9-14 are rejected under 112 2nd paragraph.

Claims 1, 15, 23-25, 28-30 are rejected under 102(b).

Claims 2-9-14, 16, 17-22, 26-27, and 31-32 are rejected under 103(a).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 15, and 28 in current application (App. # 10/644422) is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3, and 7 of a U.S. Patent No. # 6,754,117). Although the conflicting claims are not identical, they are not patentably distinct from each other.

As per claim 1 in current application (App. # 10/644422):

A memory module for a memory system, comprising:

a plurality of memory devices [same as plurality of memory device in current patent]; and a memory hub, [same as memory hub in current patent] comprising:

a link interface for receiving memory requests for access to at least one of the memory devices [same as the link interface current patent];

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices [same as the memory device interface coupled to the memory device in current patent];

a switch for selectively coupling the link interface and the memory device interface [same as the memory controller in current patent. the memory controller is coupled to the link interface and memory device interface and directs/redirects memory request to different memory devices]; and

a memory hub diagnostic engine coupled to the switch for coupling to the link interface and the memory device interface to perform diagnostic testing of the memory system, the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing and to receive diagnostic testing commands [same as the memory hub diagnostic engine; although, there is no maintenance port recited, the self-test module is "responsive to a request to test" (diagnostic testing commands) and as per claim 7 in the patent the self-test module also allows "information identifying the defective

memory...to be transferred" from it (provide access to the results). Thus a maintenance port/interface is inherent to provide these capabilities].

As per claim 15 in current application (App. # 10/644422):

A memory system for use in a computer system, the memory system comprising:

a plurality of memory modules, each module comprising:

a plurality of memory devices [same as plurality of memory device in current patent]; and

a memory hub [same as memory hub in current patent], comprising:

a link interface for receiving memory requests for access to at least one of the memory devices [same as the link interface current patent];

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices [same as the memory device interface coupled to the memory device in current patent]; and

a switch for selectively coupling the link interface and the memory device interface [same as the memory controller in current patent. the memory controller is coupled to the link interface and memory device interface and directs/redirects memory request to different memory devices];

a memory bus to which the memory modules are coupled by the respective link interfaces [inherent in current patent.]; and

a memory hub system diagnostic engine coupled to the switches of each module for coupling to the link interface and the memory device interfaces of the memory modules to perform diagnostic testing of the memory system, the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing and to receive diagnostic testing commands [same as the memory hub diagnostic engine; although, there is no maintenance port recited, the self-test module is "responsive to a request to test" (diagnostic testing commands) and as per claim 7 in the patent the self-test module also allows "information identifying the defective memory...to be transferred" from it (provide access to the results). Thus a maintenance port/interface is inherent to provide these capabilities].

As per claim 28 in current application (App. # 10/644422):

A method for performing diagnostic testing of a hub-based memory system, comprising:

providing diagnostic testing commands to a diagnostic engine located on the memory hub, the diagnostic engine having a maintenance port through which the diagnostic testing commands are coupled [same as the self-test module in current patent where it responsive to a request to test (providing diagnostic testing commands). A maintenance port/interface is inherent to provide this capability];

executing the diagnostic testing [same as the self-test module in current patent where it is responsive to the request (execute the diagnostic testing)]; and

monitoring results of the diagnostic testing of the memory system through the maintenance port of the diagnostic engine [as per claim 7 in the patent the self-test module also

allows "information identifying the defective memory...to be transferred" from it (provide access to the results). Thus a maintenance port/interface is inherent to provide this capability].

As per claim 1 in Patent (# 6,754,117):

A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a self-test module coupled to at least one of the memory devices, the self-test module being responsive to a request to test at least one of the memory devices, the self-test module further being operable to identify defective memory locations of the memory devices; and

a repair module coupled to the self-test module and at least one of the memory devices, the repair module being responsive to memory requests to defective memory locations of the memory devices to redirect the memory requests to non-defective memory locations of the memory devices.

As per claim 3 in Patent (# 6,754,117):

The memory module of claim 1 wherein the memory module further comprises:

a link interface for receiving memory requests to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices; and

a memory controller coupled to the link interface and the memory device interface and the repair module, the memory controller being operable to generate and couple memory requests from the link interface to the memory device interface by utilizing the repair module to redirect memory requests to defective locations of the memory devices to non-defective locations of the memory devices.

As per claim 7 in Patent (# 6,754,117):

The memory module of claim 1 wherein information identifying the defective memory locations of the memory devices is transferred from the self-test module to the repair module.

Claim Rejections - 35 USC § 112, 2nd Paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites "a link interface" in the last limitation, however a link interface is already claimed in the first limitation. The Examiner is unable to determine whether this link interface is the same interface claimed in the first limitation or another interface. The applicant also recites "memory device interface controller". The Examiner is unable to determine whether the applicant meant the "memory device interface" in the second limitation. For the purposes of art rejection and compact prosecution, the Examiner view "a link interface" as a separate interface

and "memory device interface controller" as "memory device interface". Claims 10-14 inherit this rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language

Claims 1 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeddeloh (United States Patent No. 6,085,339).

As per claim 1, Jeddeloh discloses:

A memory module for a memory system, comprising:

a plurality of memory devices [column 3, line 16: memory banks]; and

a memory hub [column 3, line 13: memory controller], comprising:

a link interface for receiving memory requests for access to at least one of the memory devices [column 4, lines 1-3: processor bus];

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices [column 5, line 12];

a switch for selectively coupling the link interface and the memory device interface [column 4, lines 15-40: processor]; and

a memory hub diagnostic engine [column 4, line 61: error detection module] coupled to the switch for coupling to the link interface and the memory device interface to perform diagnostic testing of the memory system [column 4, lines 61-62: perform error detection scheme], the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing [column 5, lines 33-36: passes data back to the processor] and to receive diagnostic testing commands [column 5, lines 13-17: responds to received request through conventional circuitry].

As per claim 15, Jeddeloh discloses:

A memory system for use in a computer system, the memory system comprising:

a plurality of memory modules, each module comprising:

a plurality of memory devices [column 3, line 16: memory banks]; and

a memory hub [column 3, line 13: memory controller], comprising:

a link interface for receiving memory requests for access to at least one of the memory devices [column 4, lines 1-3: processor bus];

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices [column 5, line 12]; and

a switch for selectively coupling the link interface and the memory device interface [column 4, lines 15-40: processor];

a memory bus to which the memory modules are coupled by the respective link interfaces [column 5, lines 12-13 and figure 1, reference 85 connection]; and

a memory hub system diagnostic engine [column 4, line 61: error detection module] coupled to the switches of each module for coupling to the link interface and the memory device interfaces of the memory modules to perform diagnostic testing of the memory system [column 4, lines 61-62: perform error detection scheme], the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing [column 5, lines 33-36: passes data back to the processor] and to receive diagnostic testing commands [column 5, lines 13-17: responds to received request through conventional circuitry].

Claims 1, 15, 23-25, 28-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (United States Patent Publication No. 2002/0194558).

As per claim 1, Wang discloses:

A memory module for a memory system, comprising:

a plurality of memory devices [Figure 5: multiple memory array]; and

a memory hub [Figure 1: memory controller], comprising:

a link interface for receiving memory requests for access to at least one of the memory devices [Figure 1, reference 110-113, para 0080 and para 0082: reading and writing to memory signal (memory request access)];

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices [Figure 1, para 0080: reading and writing signal from FSM to memory ram];

a switch for selectively coupling the link interface and the memory device interface [Figure 5 and para 0092]; and

a memory hub diagnostic engine [Figure 1 and para 0080: FSM controls BIST operation for memory] coupled to the switch for coupling to the link interface and the memory device interface to perform diagnostic testing of the memory system [Figure 1 and para 0080: FSM controls BIST operation for memory], the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing and to receive diagnostic testing commands [Figure 1, reference 113 and 116-119: pins to provide access to result and to receive commands, there must be a port for these pins go through].

As per claim 15, Wang discloses:

A memory system for use in a computer system, the memory system comprising:

a plurality of memory modules, each module comprising:

a plurality of memory devices [Figure 5: multiple memory array]; and

a memory hub [Figure 1: memory controller], comprising:

a link interface for receiving memory requests for access to at least one of the memory devices [Figure 1, reference 110-113, para 0080 and para 0082: reading and writing to memory signal (memory request access)];

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices [Figure 1, para 0080: reading and writing signal from FSM to memory ram]; and

a switch for selectively coupling the link interface and the memory device interface [Figure 5 and para 0092];

a memory bus to which the memory modules are coupled by the respective link interfaces [Figure 1: connection (bus) between memory modules]; and

a memory hub system diagnostic engine [Figure 1 and para 0080: FSM controls BIST operation for memory] coupled to the switches of each module for coupling to the link interface and the memory device interfaces of the memory modules to perform diagnostic testing of the memory system [Figure 1 and para 0080: FSM controls BIST operation for memory], the diagnostic engine having a maintenance port to provide access to results of the diagnostic testing and to receive diagnostic testing commands [Figure 1, reference 113 and 116-119: pins to provide access to result sand to receive commands, there must be a port for these pins go through].

As per claim 23, Wang discloses:

A method for performing diagnostic testing on a hub-based memory system having a memory hub, comprising:

coupling diagnostic testing commands to a diagnostic engine located on the memory hub, the diagnostic engine having a maintenance port through which the diagnostic testing commands

are coupled [Figure 1, reference 113 and 116-119: pins to provide access to result and to receive commands, there must be a port for these pins go through];

translating the diagnostic testing commands into control signals [Figure 5 and para 0092: the FSM accepts inputs (commands) and generates memory control signals];

coupling the control signals from the diagnostic engine to the hub-based memory system to execute diagnostic testing [Figure 1, reference 103 and para 0036: FSM generates control signals (memory commands) based on the inputs]; and

monitoring results of the diagnostic testing of the memory system through the maintenance port of the diagnostic engine [Figure 1, reference 113 and 116-119: pins to provide access to result and to receive commands].

As per claim 24, Wang discloses:

The method of claim 23, further comprising storing the diagnostic testing in a test memory coupled to the diagnostic engine [Figure 13 and para 0013: the diagnostic testing is written in the test memory which is coupled to the diagnostic engine (FSM)] and wherein monitoring results of the diagnostic testing comprises access the test memory through the maintenance port to retrieve the results [Figure 1, reference 113 and 116-119: pins to provide access to result].

As per claim 28, Wang discloses:

A method for performing diagnostic testing of a hub-based memory system, comprising:

providing diagnostic testing commands to a diagnostic engine located on the memory hub, the diagnostic engine having a maintenance port through which the diagnostic testing commands are coupled [Figure 5 and para 0092: the FSM accepts inputs (commands) and generates memory control signals];

executing the diagnostic testing [Figure 5 and para 0092: the FSM accepts inputs (commands) and generates memory control signals to execute diagnostic testing]; and

monitoring results of the diagnostic testing of the memory system through the maintenance port of the diagnostic engine [Figure 1, reference 113 and 116-119: pins to provide access to result and to receive commands].

As per claim 29, Wang discloses:

The method of claim 28, further comprising storing the diagnostic testing in a test memory coupled to the diagnostic engine [Figure 13 and para 0013: the diagnostic testing is written in the test memory which is coupled to the diagnostic engine (FSM)] and wherein monitoring results of the diagnostic testing comprises access the test memory through the maintenance port to retrieve the results [Figure 1, reference 113 and 116-119: pins to provide access to result].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 9, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558) and further in view of Kanapathippillai (United States Patent No. 6,732,203).

As per claim 2, Wang discloses:

The memory module of claim 1 wherein the memory hub diagnostic engine comprises:

a maintenance port interface to translate diagnostic testing commands into control signals for the memory hub diagnostic engine [Figure 5 and para 0092: the FSM accepts inputs (commands) and generates memory control signals];

a pattern generator coupled to the maintenance port interface to generate data patterns for the diagnostic testing in response to receiving control signals from the maintenance port interface [Figure 1, reference 106 and para 0082: data generator];

a sequencer coupled to the maintenance port interface to access the memory devices, the sequencer generating memory commands based on the control signals received from the maintenance port interface [Figure 1, reference 103 and para 0036: FSM generates control signals (memory commands) based on the inputs]

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch.

Wang does not disclose:

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch.

Kanapathippillai discloses:

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch [Figure 27 and 33A:column 54, lines 36-45: reconfigurable memory controller (switch) performs the same function as a switch take data and command signals from the BIST controller through an interface port].

Both Wang and Kanapathippillai disclose memory module systems where controllers perform diagnostic testing of memory. Wang does not disclose having a separate and distinct switch interface coupled the maintenance port interface to provide data and control to the switch. Wang discloses a system where the switching is performed by the FSM—which also performs the function of the sequencer and contains the maintenance port. Kanapathippillai's discloses a system for testing memory that utilizes a separate switch (with interface) from the diagnostic test engine to handle data and control for the memory. Having a separate switch allows for modularity, it frees up the FSM to perform specific task instead of handling the switching and routing of data and control. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to a separate switch with interface as taught in Kanapathippillai into the system of Wang for a more efficient memory diagnostic system utilizing memory.

As per claim 9, Wang discloses:

A memory hub for a hub-based memory system having a plurality of memory devices, the memory hub comprising:

a link interface for receiving memory requests for access to at least one memory device of the memory system [Figure 1, reference 110-113, para 0080 and para 0082: reading and writing to memory signal (memory request access)];

a memory device interface for coupling to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices [Figure 1, para 0080: reading and writing signal from FSM to memory ram];

a maintenance bus interface for receiving diagnostic testing commands and translating the same into control signals to perform diagnostic testing of the hub-based memory system [Figure 5 and para 0092: the FSM accepts inputs (commands) and generates memory control signals], the maintenance bus interface further providing access to results of the diagnostic testing [Figure 1, reference 113 and 116-119: pins to provide access to result sand to receive commands];

a pattern generator coupled to the maintenance bus interface to generate data patterns for the diagnostic testing in response to receiving control signals from the maintenance bus interface [Figure 1, reference 106 and para 0082: data generator];

a sequencer coupled to the maintenance bus interface to generate memory commands for accessing the plurality of memory devices based on the control signals received from the maintenance bus interface [Figure 1, reference 103 and para 0036: FSM generates control signals (memory commands) based on the inputs]; and

a link interface and memory device interface controller coupled to the maintenance bus interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the link and memory device interfaces.

Wang does not disclose:

a link interface and memory device interface controller coupled to the maintenance bus interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the link and memory device interfaces.

Kanapathippillai discloses:

a link interface and memory device interface controller coupled to the maintenance bus interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the link and memory device interfaces [Figure 27 and 33A:column 54, lines 36-45: reconfigurable memory controller (switch with a link interface) take data and command signals from the BIST controller through an interface port and provides the data and commands to the memory clusters through another interface].

Both Wang and Kanapathippillai disclose memory module systems where controllers perform diagnostic testing of memory. Wang does not disclose having a separate and distinct interface coupled the maintenance port interface to provide data and control to the link and memory interfaces. Wang discloses a system where the interface is in the FSM. Kanapathippillai's discloses a system for testing memory that utilizes a separate link interface (switch with interface) from the diagnostic test engine to handle data and control for the memory.

Having a separate link allows for modularity, it frees up the FSM to perform specific task instead of handling the switching and routing of data and control. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to a separate link interface as taught in Kanapathippillai into the system of Wang for a more efficient memory diagnostic system utilizing memory.

As per claim 17, Wang discloses:

The memory system of claim 15 wherein the memory hub diagnostic engine comprises:

a maintenance port interface to translate diagnostic testing commands into control signals for the memory hub diagnostic engine [Figure 5 and para 0092: the FSM accepts inputs (commands) and generates memory control signals];

a pattern generator coupled to the maintenance port interface to generate data patterns for the diagnostic testing in response to receiving control signals from the maintenance port interface [Figure 1, reference 106 and para 0082: data generator];

a sequencer coupled to the maintenance port interface to access the memory devices, the sequencer generating memory commands based on the control signals received from the maintenance port interface [Figure 1, reference 103 and para 0036: FSM generates control signals (memory commands) based on the inputs]; and

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch.

Wang does not disclose:

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch.

Kanapathippillai discloses:

a switch interface coupled to the maintenance port interface, the pattern generator and the sequencer to provide control signals, pattern data, and memory commands to the switch [Figure 27 and 33A:column 54, lines 36-45: reconfigurable memory controller (switch) performs the same function as a switch take data and command signals from the BIST controller through an interface port].

Both Wang and Kanapathippillai disclose memory module systems where controllers perform diagnostic testing of memory. Wang does not disclose having a separate and distinct switch interface coupled the maintenance port interface to provide data and control to the switch. Wang discloses a system where the switching is performed by the FSM—which also performs the function of the sequencer and contains the maintenance port. Kanapathippillai's discloses a system for testing memory that utilizes a separate switch (with interface) from the diagnostic test engine to handle data and control for the memory. Having a separate switch allows for modularity, it frees up the FSM to perform specific task instead of handling the switching and routing of data and control. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to a separate switch with interface as taught in Kanapathippillai into the system of Wang for a more efficient memory diagnostic system utilizing memory.

Claims 3, 10, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Cheung (United States Patent Publication No. 2004/0216018).

As per claim 3, Wang does not disclose:

The memory module of claim 1, further comprising a *DMA engine coupled to the switch to generate memory commands for the memory devices to execute diagnostic testing.*

Cheung discloses:

The memory module of claim 1, further comprising a DMA engine coupled to the switch to generate memory commands for the memory devices to execute diagnostic testing [Figures 2 & 3 and para 0010: DMA control (engine) coupled to the switch (channel array controller) to execute testing].

Both Wang and Cheung disclose memory module systems where controllers perform diagnostic testing of the devices. Wang does not disclose having a DMA engine generating memory commands. Cheung does explicitly disclose this feature in his invention. Having a separate DMA engine to generate commands for the testing can the CPU and memory controller from having to handle transfer and communication. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate DMA control as taught in Cheung into the system of Wang for a more efficient memory diagnostic system utilizing memory controllers.

As per claim 10, Wang does not disclose:

The memory hub of claim 9, further comprising a *DMA engine coupled to the link interface, the memory device interface and the maintenance bus interface to generate memory commands for the memory devices of the memory system to execute diagnostic testing in accordance with control signals from the maintenance bus interface.*

Cheung discloses:

The memory hub of claim 9, further comprising a DMA engine coupled to the link interface, the memory device interface and the maintenance bus interface to generate memory commands for the memory devices of the memory system to execute diagnostic testing in accordance with control signals from the maintenance bus interface [Figures 1, 2 & 3 and para 0010: DMA control (engine) coupled to the link interface (Fig. 1: connection between DMA controller and CPU), memory device interface (Fig. 1, reference 40: connection between DMA and module units), and maintenance bus interface (Fig. 2: connection between DMA and bus interface unit (para 0016) to execute testing].

Both Wang and Cheung disclose memory module systems where controllers perform diagnostic testing of the devices. Wang does not disclose having a DMA engine generating memory commands. Cheung does explicitly disclose this feature in his invention. Having a separate DMA engine to generate commands for the testing can the CPU and Memory controller from having to handle transfer and communication. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate DMA control as taught in Cheung

into the system of Wang for a more efficient memory diagnostic system utilizing memory controllers.

Claim 16 contains the same subject matter as claim 3. Claim 16 is just the "memory system" interpretation of claim 3. Thus, claim 3 will be used as an example rejection for claim 16.

Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Maekawa (United States Patent Publication No. 6,351,834).

As per claim 4, Wang does not disclose:

The memory module of claim 1 wherein the link interface comprises transmitter and receiver *logic having adjustable timing and voltage levels, the timing and voltage levels adjusted according to control signals generated by the memory hub diagnostic engine.*

Maekawa discloses:

The memory module of claim 1 wherein the link interface comprises transmitter and receiver logic having adjustable timing [column 3, lines 54-59] and voltage levels [column 3, lines 47-50], the timing and voltage levels adjusted according to control signals generated by the memory hub diagnostic engine [column 3, lines 54-59 and column 4, lines 54-60: voltage level and timing levels are adjusted according to controller information].

Both Maekawa and Wang disclose computer system of testing semiconductor devices (memory). While Wang does not explicitly disclose having adjustable timing and voltage levels in his system, Maekawa does disclose theses two limitations. The use of adjustable timing and voltage levels allows for the user to vary the type of test that can be performed on the device. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate adjustable timing and voltage levels as taught in Maekawa into the system of Wang to expand testing options.

Claim 11 contains the same subject matter as claim 4. Claim 11 is just the "memory hub" interpretation of claim 4. Thus, claim 4 will be used as an example rejection for claim 11.

Claim 18 contains the same subject matter as claim 4. Claim 18 is just the "memory system" interpretation of claim 4. Thus, claim 4 will be used as an example rejection for claim 18.

Claims 5, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Hassoun (United States Patent Publication No. 6,487,648).

As per claim 5, Wang does not disclose:

The memory module of claim 1 wherein the memory device interface comprises output buffers having *adjustable slew rate and drive strength, the slew rate and drive strength adjusted according* to control signals generated by the memory hub diagnostic engine.

Hassoun discloses:

The memory module of claim 1 wherein the memory device interface comprises output buffers having adjustable slew rate and drive strength, the slew rate and drive strength adjusted according to control signals generated by the memory hub diagnostic engine [column 14, lines 40-42: slew rate and drive strength are controlled (adjustable)].

Wang does not explicitly disclose having adjustable slew rate and drive strength in his system, Hassoun does disclose these two limitations. The use of adjustable slew rate and drive strength allows for the user to manage the quality of the signal during testing. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate adjustable slew rate and drive strength as taught in Hassoun into the system of Wang to manage the quality of the system.

Claim 12 contains the same subject matter as claim 5. Claim 12 is just the "memory hub" interpretation of claim 5. Thus, claim 5 will be used as an example rejection for claim 12.

Claim 19 contains the same subject matter as claim 5. Claim 19 is just the "memory system" interpretation of claim 5. Thus, claim 5 will be used as an example rejection for claim 19.

Claims 6, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Kanapathippillai (United States Patent No. 6,732,203).

As per claim 6, Wang does not explicitly disclose:

The memory module of claim 1 wherein the maintenance port of the memory hub diagnostic engine comprises a port compatible *with a JTAG standard.*

Kanapathippillai discloses:

The memory module of claim 1 wherein the maintenance port of the memory hub diagnostic engine comprises a port compatible with a JTAG standard [column 52, lines 40-41: JTAG port on a debugging system].

Both Kanapathippillai and Wang disclose systems of testing memory. Wang does not explicitly disclose if the maintenance port in the diagnostic engine is compatible with JTAG standards. While Kanapathippillai does explicitly disclose the debugger (diagnostic engine) has a JTAG compatible port. The use of JTAG is well known in the art and having a JTAG compatible port allows for the diagnostic engine to test devices with JTAG ports—which more and more devices are designed with. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a JTAG compatible port as taught in Kanapathippillai into the system of Wang to create a testing system that can test devices with JTAG ports.

Claim 13 contains the same subject matter as claim 6. Claim 13 is just the "memory hub" interpretation of claim 6. Thus, claim 6 will be used as an example rejection for claim 13.

Claim 20 contains the same subject matter as claim 6. Claim 20 is just the "memory system" interpretation of claim 6. Thus, claim 6 will be used as an example rejection for claim 20.

Claims 7, 14, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Ku (United States Patent Publication No. 2002/0199136).

As per claim 7, Wang does not explicitly disclose:

The memory module of claim 1 wherein the maintenance port of the memory hub diagnostic engine comprises port compatible with a *System Management Bus standard.*

Ku discloses:

The memory module of claim 1 wherein the maintenance port of the memory hub diagnostic engine comprises port compatible with a System Management Bus standard [para 0021: communication link is SMBus].

Both Ku and Wang disclose systems of testing. Wang does not explicitly disclose if the maintenance port in the diagnostic engine is compatible with SMBus standards. However, Ku does explicitly disclose the BIST module (diagnostic engine) has an SMBus compatible port. The use of SMBus is well known in the art and having an SMBus compatible port allows for the diagnostic engine to test devices with SMBus standards. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a SMBus compatible port as

taught in Ku into the system of Wang to create a testing system that can test devices with SMBus standard.

Claim 14 contains the same subject matter as claim 7. Claim 14 is just the "memory hub" interpretation of claim 7. Thus, claim 7 will be used as an example rejection for claim 14.

Claim 21 contains the same subject matter as claim 7. Claim 21 is just the "memory system" interpretation of claim 7. Thus, claim 7 will be used as an example rejection for claim 21.

Claims 8 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Kim (United States Patent No. 6,205,564).

As per claim 8, Wang does not disclose:

The memory module of claim 1 wherein the plurality of memory devices comprises a plurality of *synchronous random access memory devices*.

Kim discloses:

The memory module of claim 1 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices [column 5, lines 66-67: SRAM].

Both Kim and Wang disclose computer systems of testing RAM. Wang does not explicitly disclose the type of RAM used in his system, however Kim discloses the use of

Synchronous RAM. The use of Synchronous RAM is well known in the art since Synchronous RAM has greater speed and lower latency. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate synchronous RAM as taught in Kim into the system of Wang to improve performance.

Claim 22 contains the same subject matter as claim 8. Claim 22 is just the "memory system" interpretation of claim 8. Thus, claim 8 will be used as an example rejection for claim 22.

Claims 25 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Kanapathippillai (United States Patent No. 6,732,203).

As per claim 25, Wang does not disclose discloses:

The method of claim 23 wherein coupling the control signals from the diagnostic engine to the hub-based memory system to execute diagnostic testing comprises coupling the control signals *to memory controllers of the memory hub* to be provided to memory devices of the hub-based memory system.

Kanapathippillai discloses:

coupling the control signals *to memory controllers of the memory hub* to be provided to memory devices of the hub-based memory system [Figure 27 and 33A:column 54, lines 36-45:

reconfigurable memory controller receiving control signals from the BIST controller to the memory blocks]

Both Wang and Kanapathippillai disclose memory module systems where controllers perform diagnostic testing of memory. The memory BIST controller in Wang is viewed as a memory hub in the broadest interpretation. However, in Wang's system, the memory controller (hub) does not disclose having a separate and distinct memory controller in it. The FSM performs the function of a memory controller in that it accepts commands and data and performs an action accordingly. Kanapathippillai's discloses a system for testing memory that utilizes a separate controller within a hub. Having a separate controller to perform specific tasks allows for modularity, it frees up the FSM to perform specific task. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to a separate controller with interface as taught in Kanapathippillai into the system of Wang for a more efficient memory diagnostic system utilizing memory.

Claim 30 contains the same subject matter as claim 25. Claim 30 is just the "memory system" interpretation of claim 25. Thus, claim 25 will be used as an example rejection for claim 30.

Claims 26-27 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (United States Patent Publication No. 2002/0194558), and further in view of Hassoun (United States Patent No. 6,487,648).

As per claim 26, Wang does not discloses:

The method of claim 23 wherein coupling the control signals from the diagnostic engine to the hub-based memory system to execute diagnostic testing comprises coupling the control signals to link interfaces of the memory *hub to monitor the link interfaces.*

Hassoun discloses:

The method of claim 23 wherein coupling the control signals from the diagnostic engine to the hub-based memory system to execute diagnostic testing comprises coupling the control signals to link interfaces of the memory hub to monitor the link interfaces [column 14, lines 60-67: testing system monitors voltage on a pad (link interface) if selected].

While Wang does not disclose having the testing system monitor the link interfaces, Hassoun does disclose this limitation. Having the link interfaces monitored allows for a guaranteed signal [column 15, lines 2-3]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate monitoring link interfaces as taught in Hassoun into the system of Wang for guaranteed quality of signals on the interfaces.

As per claim 27, Hassoun discloses:

The method of claim 26 wherein coupling the control signals to link interfaces of the memory hub to monitor the link interfaces comprises coupling control signals to adjust slew rate or drive strength of the link interfaces [column 14, lines 40-42: slew rate and drive strength are controlled (adjustable)].

Claim 31 contains the same subject matter as claim 26. Claim 31 is just the "method for performing...having a hub-based memory system" interpretation of claim 26. Thus, claim 26 will be used as an example rejection for claim 31.

Claim 32 contains the same subject matter as claim 27. Claim 32 is just the "method for performing...having a hub-based memory system" interpretation of claim 27. Thus, claim 27 will be used as an example rejection for claim 32.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack W. Szeto whose telephone number is (571) 272-1537. The examiner can normally be reached on M-F 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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